

# Cell Library Development Methodology for Throughput Enhancement of Character Projection Equipment\*

Makoto SUGIHARA<sup>†</sup>, Member, Taiga TAKATA<sup>††</sup>, Kenta NAKAMURA<sup>††</sup>, Ryoichi INANAMI<sup>†††</sup>, Hiroaki HAYASHI<sup>††††</sup>, Katsumi KISHIMOTO<sup>††††</sup>, Tetsuya HASEBE<sup>††††</sup>, Yukihiko KAWANO<sup>††††</sup>, Nonmembers, Yusuke MATSUNAGA<sup>††</sup>, Kazuaki MURAKAMI<sup>††</sup>, Members, and Katsuya OKUMURA<sup>†††††</sup>, Nonmember

**SUMMARY** We propose a cell library development methodology for throughput enhancement of character projection equipment. First, an ILP (Integer Linear Programming)-based cell selection is proposed for the equipment for which both of the CP (Character Projection) and VSB (Variable Shaped Beam) methods are available, in order to minimize the number of electron beam (EB) shots, that is, time to fabricate chips. Secondly, the influence of cell directions on area and delay time of chips is examined. The examination helps to reduce the number of EB shots with a little deterioration of area and delay time because unnecessary directions of cells can be removed. Finally, a case study is shown in which the numbers of EB shots are shown for several cases.

**key words:** cell library, character projection, electron beam, EB shots, throughput, optimization, integer linear programming

## 1. Introduction

In the recent fabrication of semiconductor devices, quite various devices are produced while most of them result in small production volumes. The small production volumes lead to rises of the prices of products because the expensive investment made in the photomask sets must be redeemed by passing on their prices. The prices of photomasks have a great influence on the prices of semiconductor devices. The prices of photomasks increase rapidly as the transistor integration advances.

Electron Beam Direct Writing (EBDW) can draw patterns onto wafers masklessly or quasi-masklessly[4], [6]. The throughput of the conventional EBDW equipment which adopt the *variable shaped beam* (VSB) method[5] are, however, extremely low. In the VSB method, exposed patterns are divided into a large number of small rectangular and triangular shapes to draw them as shown in the left of Figure 1. In this figure, Letter “E” is divided into four rectangles and consequently needs four “EB shots” to be drawn. The conventional VSB equipment “shoots” rectangular and triangular shapes onto wafers and results in a large number of EB shots, which deteriorates the throughput of the equipment.

The *character projection* (CP) method is a more promising projection method in which pieces of patterns,

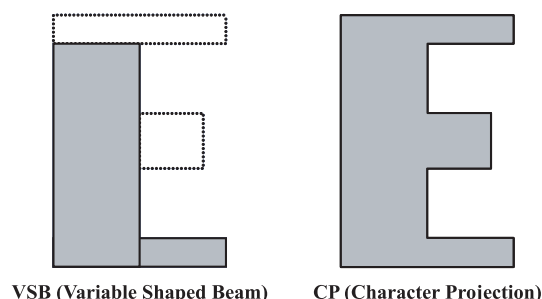


Fig. 1 VSB and CP methods.

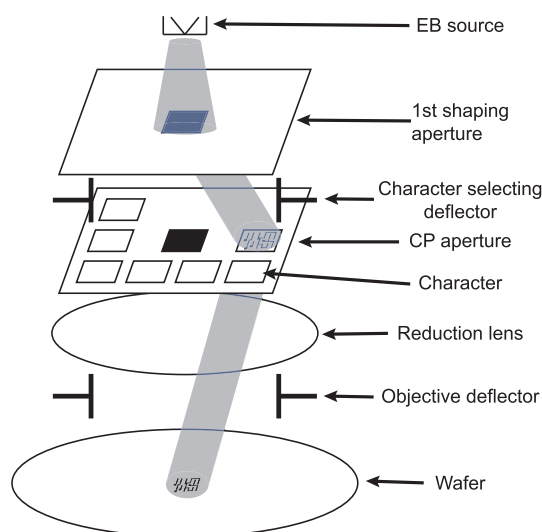


Fig. 2 Exposure equipment for character projection.

called *characters* on CP aperture masks, are *projected* onto a wafer with EB as shown in Figure 2[2], [4], [6], [7]. It is possible for the CP method to be adopted not only for maskless lithography but also for the fabrication of photomasks in the future in the sense that photomasks are developed with EB[10]. In the CP, frequently-utilized shapes in circuits are implemented as characters. *Cells* are ordinarily utilized as the basis of characters. The characters are set in an array on a CP aperture mask as shown in Figure 3. In the right of Figure 1, Letter “E” is implemented as a character of the CP method and requires only one EB shot with the CP method while four EB shots with the VSB method. The CP method is effective to decrease the number of EB shots because it can draw multiple rectangular and/or triangular shapes in a several- $\mu\text{m}$  square in one shot. The weak point of the CP method is that the number of characters available on a CP

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<sup>†</sup>The author is with ISIT, Japan.

<sup>††</sup>The authors are with Kyushu University, Japan.

<sup>†††</sup>The authors are with e-BEAM Corporation, Japan.

<sup>††††</sup>The authors are with Tokyo Electron Limited, Japan.

<sup>†††††</sup>The author is with the University of Tokyo, Japan.

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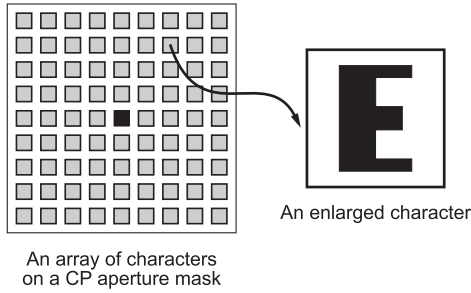


Fig. 3 A CP aperture mask.

aperture mask is limited and not all cells in a cell library can be realized on a CP aperture mask. Even if multiple CP aperture masks are used to implement all the cells, it takes a forbiddingly long time to switch CP aperture masks for setting and adjusting. In this paper, it is assumed that a single CP aperture mask is allowed to use for each layer and that the cells off the CP aperture mask are drawn by the VSB method. Our proposal aims to select an optimal set of cells to put on a CP aperture mask in order to minimize the number of EB shots. The EB shots minimization, consequently, makes the throughput of character projection equipment higher and the prices of devices lower.

Though the throughput of the CP method is much higher than that of the VSB method, it still needs to be improved because it is lower than that of the other lithography which adopts photomasks. Inanami et al. proposed a cell library development methodology for the CP[4]. In their approach, the VSB was not taken into account because the throughput of equipment comes before area, delay time and power consumption of devices. Their approach takes a long time to obtain a set of cells for the CP because logic synthesis is repeatedly done to obtain the set of cells. The set of cells consists of the small number of cells and consequently increases the area, delay time, and power consumption of devices. In this paper, we propose a cell library development methodology for the CP equipment which adopts both the CP and VSB methods. The proposed methodology minimizes the number of EB shots to draw an entire chip by selecting frequently-appeared patterns as characters of the CP method. The selected cells are placed on a CP aperture mask in order to be drawn with the CP method while the other cells, infrequently-appeared ones, are drawn with the VSB method. The optimal selection among the CP and VSB methods for each cell maximizes the throughput of the equipment. Our proposal mainly aims to build a cell library set dedicated to a product but can be easily extended to build a general cell library for multiple products. Our approach can be said as a software approach to improve the throughput of the equipment without any modification of the equipment.

The remainder of this paper is organized as follows: In Section 2, a mathematical model is shown to minimize the number of EB shots to draw an entire chip. By solving a problem instance derived from the model, an optimal cell library for the CP method can be easily sought out within short computation time. In Section 3, the influence

of cell directions on area and delay time of chips is examined experimentally. According to this experiment, the existences of cell directions hardly deteriorate delay time of chips while they deteriorate area of chips to small extent. Elimination of cell directions helps improve the throughput of the equipment. In Section 4, a case study is shown to validate our proposal. Section 5 concludes this paper with a summary.

## 2. Cell selection

In this section, a mathematical programming model is shown to select the optimal set of cells which are placed on a CP aperture mask so that the number of EB shots to draw an entire chip is minimized.

Before we describe the mathematical programming model, we briefly describe the ILP (Integer Linear Programming) to review. The ILP is a well known way to minimize loss or maximize benefit in logistics, transportation, manufacturing and so forth[9]. The goal of the ILP is to minimize (or maximize) a linear objective function on a set of integer variables, while satisfying a set of linear constraints. A typical ILP model can be described as follows:

$$\begin{aligned} \text{minimize: } & \mathbf{Ax} \\ \text{subject to: } & \mathbf{Bx} \leq \mathbf{C}, \text{ such that } \mathbf{x} \geq 0, \end{aligned} \quad (1)$$

where  $\mathbf{Ax}$  is an objective function to minimize,  $\mathbf{A}$  is an objective vector,  $\mathbf{B}$  is a constraint matrix,  $\mathbf{C}$  is a column vector of constants, and  $\mathbf{x}$  is a vector of integer variables. Efficient ILP solvers are now readily available[3].

A mathematical formulation is shown to select the optimal set of the cells which are placed on a CP aperture mask so that the number of EB shots to draw an entire chip is minimized. The problem that we examine in this section can be stated as follows.

- Given  $C$  kinds of cell objects, their reference counts  $r_1, r_2, \dots, r_C$ , their EB shots by the CP method,  $S_{CP_1}, S_{CP_2}, \dots, S_{CP_C}$ , their EB shots by VSB method,  $S_{VSB_1}, S_{VSB_2}, \dots, S_{VSB_C}$ , and a CP aperture mask capable of loading  $N_{\text{char}}$  characters, determine each cell's drawing method, the CP or VSB method, such that the total EB shots to draw the entire chip are minimized.

This problem is a typical combinatorial optimization problem and can be shown to be  $\mathcal{NP}$ -hard. However, for realistic cell libraries, the sizes of the problem instances are small. The problem instances can be solved exactly using an ILP solver within short computation time.

To model this problem, consider a chip for which  $C$  kinds of cell objects are employed. Cell  $i$  appears  $r_i$  times in the chip and is drawn with either the CP or VSB methods. If Cell  $i$  is drawn with the VSB method, let the number of EB shots to draw a cell instance of Cell  $i$  be  $S_{VSB_i}$ . Likewise, If Cell  $i$  is drawn with the CP method, let the number of EB shots to draw a cell instance of Cell  $i$  be  $S_{CP_i}$ . We introduce binary variables  $x_i$  (where  $1 \leq i \leq C$ ), which are used to determine a projection method of cells, that is the CP or

VSF method. Let  $x_i$  be a binary variable defined as follows:

$$x_i = \begin{cases} 1 & \text{if cell object } i \text{ is drawn with the CP,} \\ 0 & \text{if cell object } i \text{ is drawn with the VSB.} \end{cases}$$

The total number of EB shots  $\mathcal{S}$  to draw the entire chip is given by

$$\begin{aligned} \mathcal{S} &= \text{EB shots with the CP} + \text{EB shots with the VSB} \\ &= \sum_{i=1}^C S_{\text{CP}_i} r_i x_i + \sum_{i=1}^C S_{\text{VSB}_i} r_i (1 - x_i) \\ &= \sum_{i=1}^C (S_{\text{CP}_i} - S_{\text{VSB}_i}) r_i x_i + \sum_{i=1}^C S_{\text{VSB}_i} r_i. \end{aligned} \quad (2)$$

The second summation in the above equation does not include any variables so only the first summation is considered in the objective function of Equation (1).

Depending on the size of a cell object, the number of characters to draw a cell instance of the cell object may differ from that of the other. Cell  $i$  occupies  $c_i$  characters on a CP aperture mask. The area of the CP aperture makes a constraint on the number of characters. The following constraint, therefore, is introduced.

$$\sum_{i=1}^C c_i x_i \leq N_{\text{char}}, \quad (3)$$

where  $N_{\text{char}}$  is the maximum number of characters available on the CP aperture mask,  $c_i$  is the number of characters necessary to draw an instance of Cell  $i$  and is equivalent to  $S_{\text{CP}_i}$ .

From Equations (1), (2) and (3), a mathematical programming model for this problem can be formulated as follows.

*Objective:* Minimize  $\mathcal{S} = \sum_{i=1}^C (S_{\text{CP}_i} - S_{\text{VSB}_i}) r_i x_i$ , subject to  $\sum_{i=1}^C c_i x_i \leq N_{\text{char}}$ , i.e., every cell adopts one drawing method, the CP or VSB in conformity with the restriction of the area of the CP aperture. The minimal number of EB shots is given by  $\mathcal{S} + \sum_{i=1}^C S_{\text{VSB}_i} r_i$ .

The above model mainly aims to develop an optimal cell library set dedicated to a product but can be applied to develop a general cell library to multiple products. In order to make a cell library more general among multiple products, the reference counts of cells defined as  $r_i$  ( $1 \leq i \leq C$ ) should be set as the reference counts of cells through the total production of the multiple products. Both dedicated and general cell libraries can be easily obtained by our proposal once the reference counts of cells  $r_i$  ( $1 \leq i \leq C$ ) are given. The decision to make a cell library of a product dedicated or general is made by the following two factors.

- The cost reduction by reducing the number of EB shots with a newly developed set of CP aperture masks.
- The cost increase to newly develop the set of CP aperture masks dedicated to a product.

Even if CP aperture masks are made to dedicate to a product, the total cost for the CP aperture masks is much

cheaper than that for the photomask costs of the other lithography. The total amount of data to draw patterns on masks is a dominant factor in the costs of the both kinds of masks. The amount of data for photomasks is linear to the number of transistors while that for CP aperture masks to the number of cell objects on them. The developing cost of CP aperture masks are, therefore, much cheaper than that of photomasks. The CP with a set of CP aperture masks is still *quasi-maskless* in terms of cost.

### 3. Cell directions

There are basically four directions of cells as cell instances are physically placed as shown in Figure 4. A *basic* direction is literally a basis of the other directions. *Mirror-X*, *mirror-Y* and *mirror-XY* directions are horizontally-flipped, vertically-flipped and horizontally-and-vertically-flipped ones respectively. The patterns of these directions of a cell function must be distinguished from the other as different patterns on CP aperture masks.

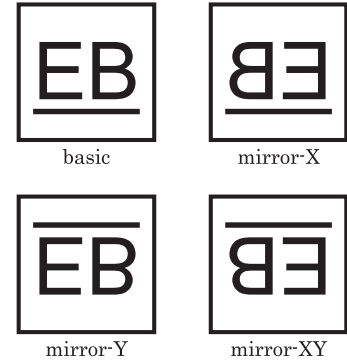


Fig. 4 Four cell directions for a cell.

In this section, we examine the influence of the existence of the cell directions on both area and delay time of a chip. We used a logic-synthesizable benchmark circuit which was a Z80-compatible microprocessor. We used a cell library whose feature size was  $0.35\mu\text{m}$ . The logic synthesis for the circuit was done with Synopsys Design Compiler[8]. Place-and-route was done with Avant! Apollo[1]. Delay times for four cell directional variations are shown in Table 1. In the table, the four-bit vectors which follow “Conf. X” denotes the existence of the four cell directions in the processes of place-and-route. The first bit of the vectors denotes the existence of the basic direction. If the direction is taken into account, the number is 1, otherwise 0. Likewise, the second, third and fourth bits denote the existences of the mirror-X, mirror-Y and mirror-XY directions respectively. The top value in each column denotes the delay time with the least area. “N/A” means that the given areas were infeasible to place and route the circuit with the place-and-route tool. For example, the least area and the delay time for the area were obtained as  $810 \times 808.5$  and  $7.09\text{ns}$  respectively in Conf. 1. The least areas for Confs. 1, 2, 3, and 4 were  $810 \times 808.5$ ,  $810 \times 808.5$ ,  $870 \times 858$ , and  $879 \times 874.5$  respectively. About 14% area increased when the mirror-Y

**Table 1** Delay times for four cell directional variations.

P&R area	Delay times for four cell directional variations [ns]. (normal,mirror-X,mirror-Y,mirror-XY)			
	Conf. 1	Conf. 2	Conf. 3	Conf. 4
	(1111)	(1010)	(1100)	(1000)
799.5 × 792	N/A	N/A	N/A	N/A
810 × 808.5	7.09	6.97	N/A	N/A
819 × 808.5	7.37	7.43	N/A	N/A
829.5 × 825	7.52	-	N/A	N/A
840 × 825	7.16	-	N/A	N/A
849 × 841.5	7.24	-	N/A	N/A
859.5 × 858	7.11	-	N/A	N/A
870 × 858	-	-	7.15	N/A
879 × 874.5	-	-	7.23	7.15
889.5 × 874.5	6.86	-	-	-
900 × 891	7.23	-	6.90	-

and the mirror-XY were forbidden. Theoretically speaking, delay time decreases under a case as place-and-route area increases. Delay time in a column of the table is expected to decrease downward but it did not. This is because the CAD tool is based on approximate algorithm. Comparing the two values of Conf. 2, 6.6% delay time increased while place-and-route area increased.

Conf. 1 is the configuration in which all the four cell directions are available and is supposed to be best with regard to area and delay time among the configurations because its design space includes design space of other configurations, that is any layout based on Confs. 2, 3 or 4 can be realized by Conf. 1. The results which the CAD tool reported don't straightforwardly reflect this supposition because the layouts obtained by the CAD tool are approximate solutions, e.g. the delay time of Conf. 2 (6.97 ns) was better than that of Conf. 1 (7.09 ns) as the place-and-route area was 810 × 808.5!

Conf. 2 is the configuration in which the horizontal flippings are removed from Conf. 1. In other words, the mirror-X and mirror-XY directions are not taken into account in Conf. 2. There was no great difference of delay times among Confs. 1 and 2. Horizontal flipping seems not to be so effective to reduce delay time and area.

Conf. 3 is the configuration in which the vertical flippings (mirror-Y and mirror-XY) are removed from Conf. 1. Experimental results show that the vertical flipping of cells had little influence on delay time of the chip and it had some influence on the area. Comparing Conf. 3 with Conf. 1, about 14% area increased. This is because the gaps between cell areas were added by eliminating vertical flipping of cells and each cell area got to own its own power and ground lines.

Conf. 4 is the configuration in which any flipping cells are forbidden and only a basic direction of cells is available. Comparing Conf. 4 with Conf. 1, the differences of the delay times were insignificant while the those of the areas were noticeable, that is about 14% area increase. This is because of the same reasons that the area of Conf. 3 increased. Comparing Conf. 4 with Conf. 3, the differences of their best delay times were insignificant while the those of their areas were about 4.2%. Horizontal flipping had some

influence on the area increase as vertical flipping was completely forbidden.

There was no big difference among delay times between the four configurations. It was experimentally validated that cell directions were not strongly relevant to the increase of delay time. The existence of vertical flipping of cells was relevant to increase of area. This was because gaps between cell areas come to arise and each cell area got to own its own power and ground lines.

#### 4. Case Study

In this section, a case study is shown for five cases to examine the relation between the number of EB shots and how to select cell objects to place on characters. The five cases are explained in Table 2. We developed the cell selection software described in Section 2 with a commercial mathematical optimization engine, ILOG CPLEX 9.0[3]. Every optimization process finished within a second.

The specification of the CP equipment for which we assumed is shown in Table 3. Two benchmark circuit was used to examine their numbers of EB shots under the five cases. The description for the benchmark circuits is shown in Table 4. Note that the cell library is from academia and comprises less kinds of cells than that from industry.

The EB shots under the five cases were sought out by solving mathematical problem instances and are shown in Table 5. In the table, the parenthesized values show the numbers of cell objects. The areas and delay times of Circuit 2 are shown in Table 6. In our experiment, areas and delay times of Circuit 1 were not examined because the benchmark circuit was not logic-synthesizable.

According to Table 5, as the number of cell objects in-

**Table 2** Target cases for experiment.

	Description
<b>Case 1:</b>	Only a basic cell direction is available. The optimal set of cells are exactly searched out by solving an ILP problem instance.
<b>Case 2:</b>	Two cell directions, that is the basic and the Mirror-Y directions, are taken into account. It is assumed that the reference count of a direction of a cell function is equal to that of the other direction of the cell function. Each direction is assigned 1/2 of available characters to. This is after the fashion of [4].
<b>Case 3:</b>	The two directions, that is the basic and Mirror-Y directions, are available in this case. Cell objects to be placed on a CP aperture mask are exactly searched with our cell selection method.
<b>Case 4:</b>	The four cell directions are available. It is assumed that the reference count of a direction of a cell function is equal to that of the other directions. Each direction is assigned 1/4 of available characters to. This is also after the fashion of [4].
<b>Case 5:</b>	The four cell directions are available. Cell objects to be placed on a CP aperture mask are exactly searched with our cell selection method.

**Table 3** Specification of CP/VSB equipment.

The maximum width and length of rectangles for VSB	3.5 $\mu$ m
The width and length of characters for CP	5 $\mu$ m
The number of characters on a CP aperture mask	400

**Table 4** Benchmark circuit.

	Circuit 1	Circuit 2
Feature size [ $\mu\text{m}$ ]	0.25	0.35
# of cell objects in the cell library (mirroring ignored)	395	395
# of mapped cell objects (mirroring ignored, 1 direction)	74	111
# of mapped cell objects (mirroring considered, 2 directions)	128	191
# of mapped cell objects (mirroring considered, 4 directions)	211	303
# of cell instances	2311	3165

**Table 5** EB shots and cell objects.

	Case 1	Case 2	Case 3	Case 4	Case 5
	# dir: 1	# dirs: 2		# dirs: 4	
Circuit 1	15268 (74)	17300	16915 (128)	30925	29733 (211)
Circuit 2	51055 (111)	69760	69589 (191)	93774	91187 (303)

**Table 6** Area and delay time of Circuit 2.

	Case 1	Cases 2 and 3	Cases 4 and 5
Area [ $\mu\text{m}^2$ ]	768,685.5	654,885	654,885
Delay time [ns]	7.15	6.97	7.09

increases, in other words, the number of cell directions increases, the number of EB shots increases. This is because the reduction of cell directions enables more cell functions to be on a CP aperture mask and to be projected with the CP. The area of Circuit 2 under Case 1 was largest among the five cases as shown in Table 6 because only a single direction, that is a basic direction, was adopted for place-and-route. This was because the gaps between cell areas come to arise and each cell area got to own its own power and ground lines. Theoretically speaking, the design with the four cell directions should be best among the five cases with regard to area and delay time. Similarly, the design with the two cell directions should be intermediate. The experimentally obtained values of areas don't reflect this theory. The delay time of Circuit 2 under Cases 2 and 3 was found best. This is because the CAD tool returned approximate solutions of layout and happened to result against the theory. Note that the values shown in Tables 1 and 6 are nothing more than the ones the CAD tool reported. If a design obtained with the two cell directions is better than a design obtained with the four cell directions, the design of two-cell direction may be adopted as a design of four-cell direction.

Comparing the number of EB shots of Circuit 1 under Case 4 with that under Case 5, 3.85% reduction of the number of EB shots was achieved. The difference in the numbers of EB shots caused by solving the problem instances exactly or approximately. The optimal sets of cells was selected exactly under Cases 3 and 5 while sets of cells was selected approximately under Cases 2 and 4 by assigning the equal number of characters to each directions of cells.

Comparing the number of EB shots of Circuit 1 under Case 2 with that under Case 4, 44% reduction of EB shots was achieved. Likewise, comparing the number of EB shots of Circuit 2 under Case 2 with that under Case 4, about 26% reduction of EB shots was achieved. It was experimentally found that the elimination of cell directions is quite effective to reduce EB shots. It was experimentally found that the

elimination of horizontal flipping reduced the much number of EB shots effectively while it has small impact on area and delay time of chips.

## 5. Conclusion

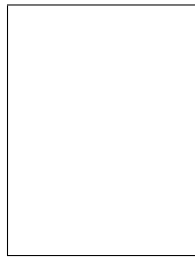
In this paper, we proposed an ILP-based cell library development methodology to reduce the number of EB shots. All optimization processes finished within a second. More than 3.85% reduction of EB shots was achieved only by distinguishing between the differently mirrored cells whose functions are identical.

We examined the influence of cell directions on both area and delay time of the circuit. It was experimentally validated that both of the horizontal and vertical flipping of cells had little influence on delay time of chips. The horizontal flipping had little influence on area while the vertical flipping had some influence on area. This examination helps which cell direction should be implemented on CP aperture masks.

The forbiddance of horizontal flipping caused little deterioration of area while 25.6% reduction of EB shots. It was found that the forbiddance of horizontal flipping was effective to reduce the number of EB shots while it deteriorated little area and delay time of chips. The forbiddance of vertical flipping caused 13.9% increase of area while it caused less than 1% increase of delay time. The forbiddance of vertical flipping should be determined with taking a tradeoff between area and EB shots into account. For many chips of the state of the art, cells are placed so "loosely" that the deterioration of area caused by forbiddance of multi directions of cells might have less impact on area. The relation between cell directions and EB shots in design of such chips should be further examined as future work.

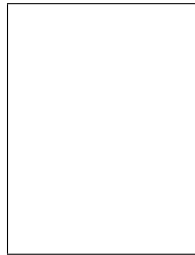
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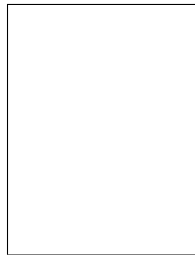


**Makoto Sugihara** was born in Tokyo, Japan in 1974. He received the B.E., M.E. and Ph.D. degrees in computer science and communication engineering from Kyushu University, Japan in 1996, 1998 and 2001, respectively. He worked for the Fujitsu Laboratories, Japan, in 1998. He was a visiting researcher at Duke University from April 2002 to March 2003. He is currently a researcher at ISIT and is also a visiting associate professor at Kyushu University. His research interest includes design and test method-

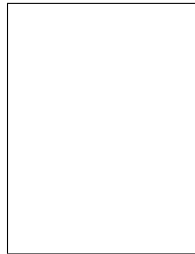
ologies as well as CAD algorithms for VLSI. He is a member of the IEEE and the IEEE Computer Society, the IEICE, and the IPSJ.



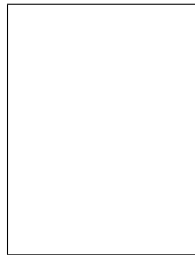
**Taiga Takata** received the B.E. degree from Kyushu University, Japan 2005. He is currently a student at the Graduate School of Information Science and Electrical Engineering, Kyushu University. His current research interests include CAD algorithms and design methodology for VLSI.



**Kenta Nakamura** was born in Kumamoto, Japan in 1978. He received the B.E. and M.E. degrees from Kyushu University in 2001 and 2003 respectively. From 2003, he has been a Ph.D. candidate at Kyushu University.



**Ryoichi Inanami** received the B.E. degree in electrical and electronic engineering from the Meijo University in 1992, and received the M.E. and D.E. degrees in electronic engineering from Nagoya University in 1994 and 1997, respectively. He joined the ULSI process engineering Laboratory, Toshiba Corporation, in 1997. He has been engaged in the research and development for electron-beam lithography. He is currently on loan to e-BEAM Corporation.



**Hiroaki Hayashi** received the B.E. and M.E. degrees from Kyushu Institute of Technology, Japan in 1985 and 1987 respectively. He is currently with Tokyo Electron Limited, Tokyo, Japan. He is also a visiting assistant professor at Yamanashi University. His research interest includes computer architecture and design methodology for ICs.



**Katsumi Kishimoto** received the B.E. degree from Kyushu Institute of Technology, Japan in 1978. After a job experience at a semiconductor design firm, he joined DAINIPPON SCREEN MFG. Co.,Ltd. in 1984. He has been engaged in the research and development of computational geometry for the laser beam writing systems. He is currently on loan to e-BEAM Corporation, Tokyo, Japan in order to develop the electron beam direct writing systems for semiconductor devices.



**Tetsuya Hasebe** received the B.E. degree from Ritsumeikan University, Japan, in 1972. He is currently with Tokyo Electron Limited, Tokyo, Japan. His research interest includes computer architecture and ASIC development.



**Yukihiro Kawano** was devoted himself to the development of dry etching systems and thermal process systems for flat panel displays at Tokyo Electron Limited. He is currently on loan to e-BEAM Corporation, Tokyo, Japan and is engaged in the development of the electron beam direct write systems for semiconductor devices.



**Yusuke Matsunaga** received B.E., M.E. and Ph.D. degrees in Electronics and Communications Engineering from Waseda University, Tokyo, Japan, in 1985, 1987 and 1997, respectively. He joined Fujitsu Laboratories in Kawasaki, Japan, in 1987 and he has been involved in research and development of the CAD for digital systems. From October 1991 to November 1992, he has been a visiting Industrial Fellow at the University of California, Berkeley, in the department of Electrical Engineering and Computer Sciences. In 2001, he joined the faculty at Kyushu University. He is currently an associate professor of Department of Computer Science and Communication Engineering. His research interest includes logic synthesis, formal verification, high-level synthesis and automatic test patterns generation. He is a member of IEEE, ACM and IPSJ.



**Kazuaki Murakami** received the B.E., M.E. and Ph.D. degrees in computer science and engineering from Kyoto University in 1982, 1984, and 1994, respectively. From 1984 to 1987, he worked for the Fujitsu Limited, where he was a computer architect of the mainframe computers. In 1987, he joined the Department of Information Systems of Kyushu University, Japan, as an assistant professor. Since 1996, he was an associate professor of the Department of Computer Science and Communication Engineering. He is currently a professor of the Department of Information Science. He is a member of the ACM, the IEEE, the IEEE Computer Society, the IPSJ, and the JSIAM.



**Katsuya Okumra** spent more than 30 years in the semiconductor process development with Toshiba, much of it in R&D. He is a professor at the research center for advanced science and technology, the university of Tokyo, Japan. Now he heads a joint private, academic and government project that aims to create minifab that is just 10% of the size and cost of today's monster plant.