A CP Mask Development Methodology for MCC Systems

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ABSTRACT

The character projection (CP) is utilized for maskless lithography and is a potential for the future photomask manufacture because the CP can project ICs faster than the point beam projection and the variable-shaped beam (VSB) projection. The drawback of the CP is its lower throughput than that of photomask-based lithography and the amortization cost of CP equipment leads to the price rise of ICs. This paper discusses a CP mask development methodology for increasing the throughput of MCC systems. The proposed methodology virtually increases the number of the logic cells which are projected with the CP. In the proposed methodology, the multiform CP masks are utilized among the column-cells for reducing the VSB projection. The experimental results show that the proposed CP mask development methodology reduced 71.3% of the number of EB shots needed for an SCC system. It also reduced 42.6% of the number of EB shots needed for the MCC system in which uniform CP masks are utilized for all column-cells.

Keywords: Character Projection, Variable Shaped Beam, Maskless Lithography, Electron Beam Direct Write, MCC Systems, Throughput, CP Masks

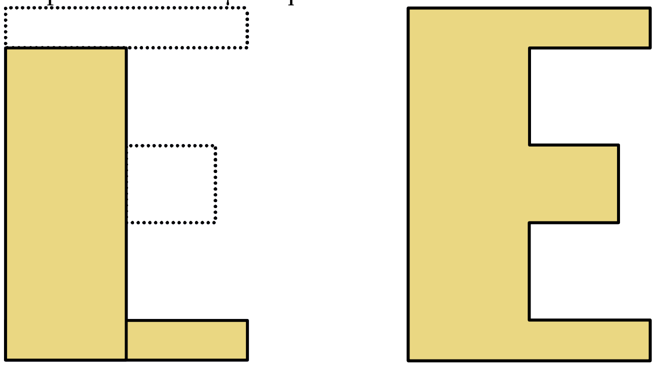
1. INTRODUCTION

In the recent fabrication for semiconductor devices, quite various semiconductor devices are manufactured while most of them result in the small production volume. The small production volume of a product leads to its price rise because the expensive investment made in the photomask set must be redeemed by passing on its price. The price of the photomask set has the great influence on the price of a semiconductor device. The photomask price increases rapidly as the transistor integration advances.

The electron beam direct write (EBDW), that is maskless lithography, can project patterns onto silicon wafers masklessly or quasi-masklessly [2,5]. The throughput of the conventional maskless lithography equipment which adopts the variable shaped beam (VSB) method introduced in [4] is, however, extremely low. In the VSB projection, exposed patterns are divided into a large number of small rectangular and triangular shapes to draw them [4] as shown in the left of Figure 1. In the left of the figure, Letter "E" is divided into four rectangles and consequently needs four electron beam (EB) shots to project. The conventional VSB equipment "shoots" a large number of rectangular and triangular shapes onto silicon wafers, which deteriorates the throughput of the VSB equipment.

The character projection (CP) lithography is the other projection method in which pieces of patterns, called characters implemented on CP masks, are projected onto a silicon wafer with electron beams as shown in Figure 2 [1,2,5,6]. The character projection (CP) lithography is a method to increase the throughput of maskless lithography as well as photomask manufacture [11,12]. In the right of Figure 1, Letter "E" is implemented as a character and requires only one EB shot with the CP while four EB shots with the VSB. Sakitani et al. developed the actual character projection equipment [6].

The throughput of the CP equipment is much higher than that of the VSB equipment because all rectangular and triangular shapes in a several-μm square can be shot at once in the CP method.



VSB (Variable Shaped Beam) CP (Character Projection)

Figure 1: EB shots with the VSB and CP methods.

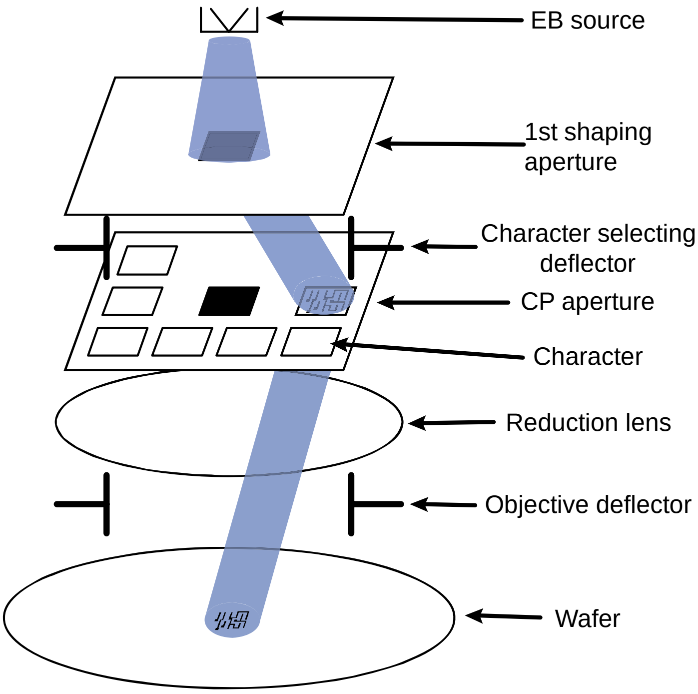


Figure 2: Character projection equipment with a single column-cell.

Logic cells are ordinarily utilized as the basis of characters. The characters are set in an array on a CP mask as shown in Figure 3. A CP mask accommodates several hundred characters which are several-μm squares. The number of characters available on a CP mask is limited to a small one and not all logic cells in a cell library can be realized on the CP mask. For example, a CP mask can accommodate only 50-70 cells in 0.35μm technology. It is quite important to select frequently-utilized logic cells in design to put on CP masks because characters on CP masks are precious resources to increase the throughput of the system. The authors proposed a CP mask optimization methodology for increasing the throughput of character projection equipment [7,9].

Several CP mask development methodologies for the CP lithography have been researched especially for single column-cell (SCC) systems [2,3,5-10]. The weak point of the SCC-based CP lithography is that not all logic cells used for an IC can be placed on a CP mask. The logic cells off the CP mask must be projected with the VSB projection. This deteriorates the throughput of the projection equipment. Even if multiple CP masks are available to implement all logic cell included in a cell library, it takes a forbiddingly long time to switch the CP masks for setting and adjusting. This paper assumes that a single CP mask is allowed for each column-cell to utilize for each layer and that the cells off the CP mask are drawn by the VSB method.

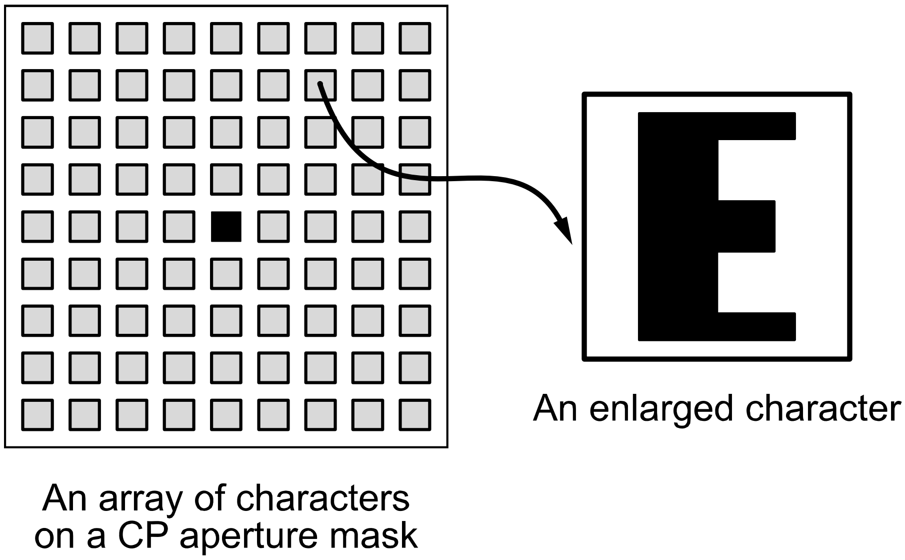


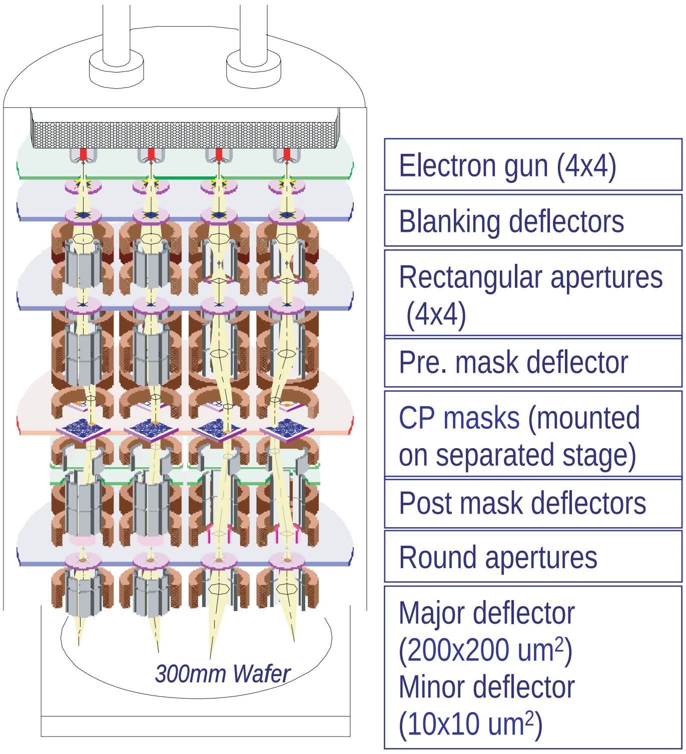
Figure 3: A CP mask.

It is natural to adopt multiple column-cells for the higher throughput of projection equipment. The multi-column-cell (MCC) system, which literally has multiple column-cells with it, is one of the solutions to the low throughput of maskless lithography systems [11,12]. It accommodates several column-cells each of which has an electron gun and a CP mask as shown in Figure 4. Parallelizing projections contributes to the increase of the throughput of the CP equipment.

This paper discusses a CP mask development methodology for increasing the throughput of MCC systems. A column-cell of the projection equipment conventionally and naively has uniform CP masks among all column-cells while it has multiform CP masks in the proposed approach. In the proposed approach, each column-cell doesn't have to finish projecting a whole IC but project its favorite parts of the IC. The remainder of the IC should be projected by the others which have the corresponding characters on their CP masks. The proposed approach virtually increases the number of logic cells implemented on a CP mask for avoiding the VSB projection as much as possible.

The remainder of this paper is organized as follows. Section 2 examines the factor to deteriorate the throughput of an SCC system. The examination clearly illustrates that the reliance of the SCC system on the VSB projection deteriorates the throughput of projection equipment. Section 3 proposes a CP mask development methodology for MCC systems in which each column-cell may have its own CP mask to project a layer of a chip. Section 4 experimentally shows that the proposed approach reduced 42.6% of the number of EB shots for an MCC system which has naive CP masks with it.

Section 5 concludes this paper with a summary.



Courtesy of ADVANTEST

Figure 4: An Advantest MCC system with 16 projection mechanisms.

2. CP MASK DEVELOPMENT FOR SINGLE-COLUMN-CELL SYSTEMS

In single-column-cell (SCC) systems, all logic cells cannot be implemented on a CP mask because of the limitation of the area of the CP mask. For SCC systems, frequently utilized logic cells are implemented on a CP mask and projected with the CP. The others logic cells off the CP mask are projected with the VSB. The authors studied the optimal cell selection methodology to put logic cells on a CP mask for SCC systems [7,9]. They developed a mathematical model in which the optimal logic cells to put on a CP mask are selected so that the number of EB shots to project an entire chip is minimized. The EB shots minimization reduces time to project an entire chip as well as the amortization cost of SCC systems. They also proposed a projection size optimization to enhance the throughput of SCC systems [10]. They reported that their projection size optimization reduced about 70% of the number of EB shots needed for the conventional projection systems. They concluded that SCC systems should be capable of configuring the electron beam size as well as the character size for enhancing the throughput of the SCC systems. The authors also proposed a technology mapping technique for increasing the throughput of character projection lithography [8]. The technique is to optimize area and the number of EB shots for ICs in the technology mapping process.

The excessive reliance of CP systems on the VSB deteriorates their throughput. Table 1 shows the numbers of EB shots to project four benchmark circuits which consist of only logic cells. All circuits were projected with the electron beams whose sizes were 5μm-squares. The authors used two cell libraries supplied from academia. The number of the cell functions included in each academic cell library is smaller than that of cell functions included in a typical commercial cell library. In the sense, the percentage of the number of EB shots projected with the CP became relatively high. The numbers of EB shots with the VSB for the four circuits account for 53.2%, 52.4%, and 35.8% of the total numbers of EB shots respectively. The projection time spent for the VSB could be reduced if the logic cell instances were projected with not the VSB but the CP.

Table 1: The numbers of EB shots with the CP and the VSB to project four benchmark circuits.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
The number of logic cell objects on a CP mask	33	51	73	98
The number of logic cell objects off a CP mask	85	113	138	34
The number of logic functions	310	310	395	395
The number of all cell objects	1240	1240	1180	1180
Feature size [μm]	0.35	0.35	0.25	0.25
The total number of EB shots	64,704	41,469	26,889	164,269
The number of EB shots with the CP	41,900 (64.8%)	24,873 (60.0%)	14,034 (52.2%)	161,062 (98.0%)
The number of EB shots with the VSB	22,804 (35.2%)	16,596 (40.0%)	12,855 (47.8%)	3,207 (2.0%)

3. CP MASK FOR MCC SYSTEMS

In the conventional and naive operation of an MCC system, it has multiple column-cells each of which has the same CP mask set as the others. If logic cells are on the CP masks, they are drawn with the CP. The other logic cells are drawn with the VSB. The example of an MCC system is shown in Figure 4. The MCC system has 16 column-cells in it and can draw 16 patterns in parallel. Figure 5 shows which ICs each column-cell draws. There are 148 ICs on the silicon wafer in the example while the MCC system can finish drawing the whole silicon wafer in projection time during which 16 ICs are drawn sequentially. The MCC system, resultantly, draws all the ICs on the silicon wafer 9.25 times faster than a single-column-cell system.

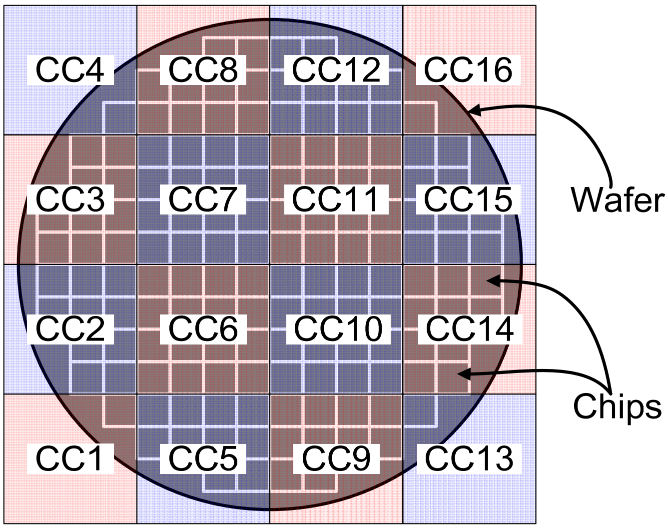


Figure 5: Division of the projection task among 16 column-cells.

In this paper, the authors propose a CP mask development methodology for MCC systems, in which multiform CP masks are given to cell-columns for increasing the number of logic cells placed on CP masks. The increased number of logic cells placed on CP masks contributes to increasing the number of cell instances which are projected with the CP. The authors think that each column-cell doesn't necessarily have to have the uniform CP masks among column-cells. Adopting multiform CP masks increases as many logic cells on CP masks as possible and avoids the VSB projection. Figure 6 shows that adopting multiform CP masks increases the number of logic cells on CP masks and decreases the number of logic cells off the CP masks.

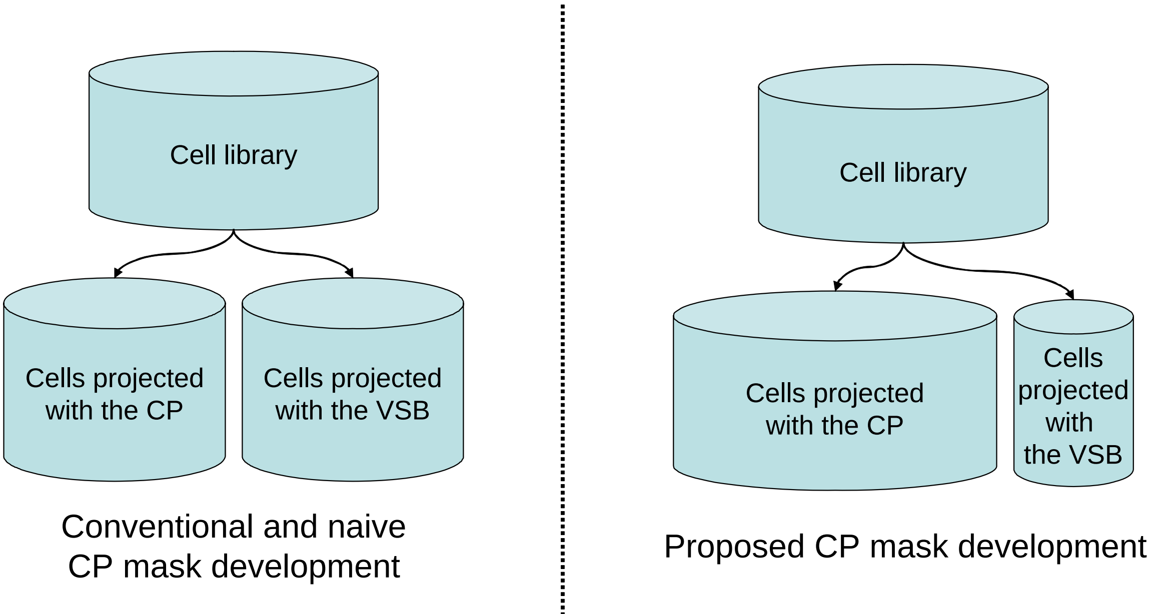


Figure 6: Logic cells virtually increased by multiform CP masks.

Figures 7 and 8 present instantial chip projections with the naive approach and the proposed one. In these instances, both MCC systems have two column-cells. Only Cell Set *A* is implemented on CP masks and projected with the CP in the naive approach while Cell Sets *A* and *B* are implemented on CP masks and projected with the CP in the proposed approach. In the naive approach, each column-cell has a CP mask for Cell Set *A*. Cell Set *A* is projected with the CP and Cell Sets *B* and *C* are projected with the VSB as shown in Figure 7. In the proposed approach, one column-cell has a CP mask for Cell Set *A* and the other has a CP mask for Cell Set *B*. Cell sets *A* and *B* are, consequently, projected with the CP and Cell Set *C* is projected with the VSB as shown in Figure 8. Our idea is to adopt multiform CP masks for a layer to reduce EB shots by increasing the number of cell objects placed on CP masks and reducing the number of cells projected with the VSB. In this example, the conventional projection draws six ICs while our projection draws seven ICs.

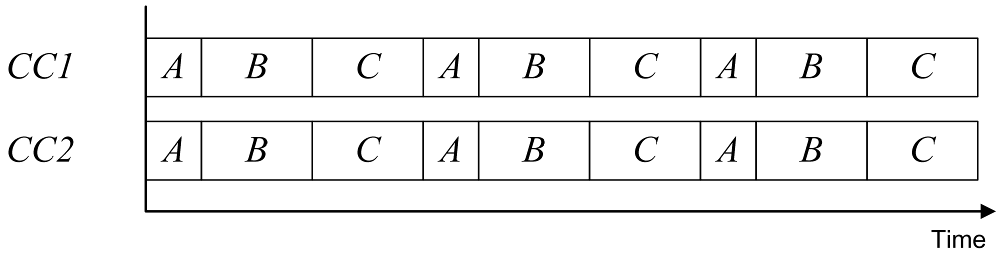


Figure 7: Chip projection with the uniform CP masks.

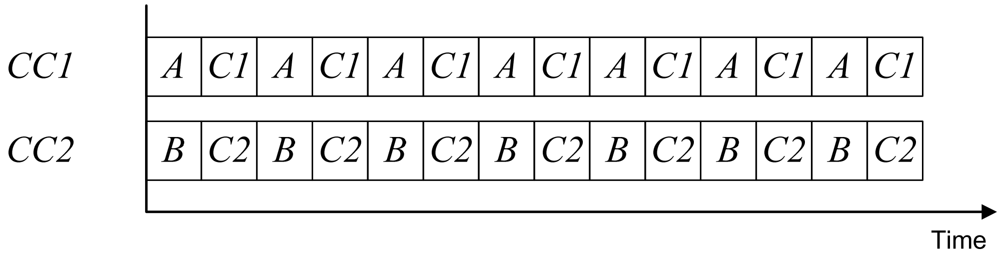


Figure 8: Chip projection with the multiform CP masks.

4. CASE STUDY

The authors examined how many EB shots it takes to project four benchmark circuits with an SCC system, an MCC system which has uniform CP masks, and an MCC system which has multiform CP masks. The four circuits are described in Table 2 and each system is described in Table 3. The authors used two cell libraries from academia. The number of cell functions included in each academic cell library is smaller than that of cell functions included in a typical commercial cell library. The numbers of EB shots to project the four benchmark circuits with each projection system are shown in Table 4. It was assumed that column-cells can project anywhere on a silicon wafer in the calculation for these numbers of EB shots. The number of EB shots by a naive MCC system is half of that of the SCC system. Only parallelizing column-cells contributed to enhancing the throughput of the projection equipment in the naive MCC system. The proposed MCC system with multiform CP masks achieved the less number of EB shots than the naive MCC system with uniform CP masks did. Increasing the number of logic cells on CP masks contributed to the reduction of EB shots. The proposed MCC system reduced 71.3% of the number of EB shots needed for the SCC system at best. It also reduced 42.6% of the number of EB shots needed for the naive MCC system at best. It was experimentally validated that multiform CP masks for MCC systems could achieve the less number of EB shots than uniform CP masks for MCC systems.

Table 2: Benchmark circuits.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
The number of cell instances	3,875	3,943	2,311	35,683
The number of logic cell objects drawn with the CP	42	66	140	98
The number of logic cell objects drawn with the VSB	76	98	71	34
The number of logic functions	310	310	395	395
The number of all cell objects	1240	1240	1580	1580
Feature size [μm]	0.35	0.35	0.25	0.25

Table 3: CP equipment specifications.

	Specification
SCC system	The system has a single-column-cell and has a CP mask for projecting each layer. The number of EB shots is obtained exactly with the approach presented in [7,9].
MCC system with uniform CP masks	The system has two column-cells and has uniform CP masks among the two column-cells. It was assumed that the column-cells can project shapes onto anywhere of a silicon wafer for simplifying the projection planning.
MCC system with multiform CP masks	The system has two column-cells and has multiform CP masks among the two column-cells. It was assumed that the column-cells can project shapes onto anywhere of a silicon wafer for simplifying the projection planning.

Table 4: The numbers of EB shots to draw each of the four benchmark circuits.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
SCC system	64,704	41,470	26,889	164,269
MCC system with uniform CP masks	32,352	20,735	13,445	82,135
MCC system with multiform CP masks	26,702	15,920	7,719	80,683

5. CONCLUSION

The authors proposed the CP mask development methodology for MCC systems. The naively-made CP mask set consists of uniform CP masks while the CP mask set based on the proposal consists of multiform CP masks as the optimal set for projecting an IC product. The experimental results reported that the proposed methodology reduced 71.3% and 23.2% of the numbers of EB shots required for an SCC system and a naive MCC system respectively. In the experiment, the authors utilized the two cell libraries from academia. The number of logic cells included in a typical commercial cell library is higher than that of the two cell libraries utilized in the experiment. In the sense, the authors think that the proposed technique can reduce much more EB shots in design of commercial ICs.

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